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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	130.1012.02	6854

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	19

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/443,160	ISAMAN, DAVID L.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *1-5 and 12-15* is/are rejected.

7)☒ Claim(s) *6-11 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/08/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2-21 remain for examination. Claims 1 has been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-5, 12-15 are rejected under 35 U.S.C. 102(a) (b) as being anticipated by Amerson et al. (5,475,823) .

3. Claims 2-5,12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view of Webb, Jr. et al. (6,360,314) .

4. As to the newly amended claim 2, the scope of amended feature of

5. "A pipeline processor...the instruction is detected without requiring computation of ...memoir address" is not different from the scope of the original language

6. "A pipeline processor...detecting an instruction...without computing...memory address".

7. Additional reasoning is provided below. The examiner would like to make one point clear, and hopefully applicant can clarify this in the next response. It is not sure whether applicant is claiming the detection of the load instruction itself without requiring the computation, or the applicant is claiming the detection of the load instruction in addition to the "without computation". According to the teaching of applicant in page 4,

lines 8-11, a pipelined microprocessor is operated more quickly , by detecting the load instruction, without having to compute the referenced memory address. Therefore, the "without compute" feature is directed to the pipeline microprocessor , not to the detection of the load instruction itself . In page 7, lines 8-10, the detection of a load instruction was done by parsing, but nowhere does applicant specification teach whether this parsing requires computation or not. In page 8, lines 20-22, page 9, lines 1-22, applicant taught a bypass to indicate to a computation stage 130 not have to compute the address referenced by the load instruction based on the same address. From the above teaching, it is clearly understood that the computation of the address referenced by the load instruction was bypassed , but it is not the detection of the load instruction. Detection of the load instruction without requiring computation is different than the detection of same address, and then, based on the determination, computation was bypassed. The examiner only found the determination of the same operand address referenced by the load with the previous store, and the computation was bypassed (see page 8, lines 20-22, page 9, line 1-22), not the detection of the instruction without requiring the computation.

8. If applicant insists that the instruction was detected without requiring the computation as in the claim is correct, can applicant show, in the next response, where in the specification that teaches the detection of the load instruction without computing ? And, it might have been a potential lack of enabling and written description problems. Applicant is welcome to provide feedback or corrections in the next response.

9. For examination purpose, the examiner takes the position based on the teaching as set forth in the page 8, lines 20-22, page 9, line 1-22. It is the determination of same operand address referenced by load and store for the purpose of bypassing the computation. Applicant is welcome to provide feedback in the next response.

10. The rejections are maintained and incorporated by reference the last Office action on 12/10/03.

11. Applicant's response filed on 03/15/01 have been fully considered but is not persuasive.

12. In the remarks, applicant argued that :

a) the access level being claimed, and examiner impermissibly reading limitations into claims;

b) Amerson must calculate the memory address;

c) Webb must calculate the address.

13. As to a) above, is applicant trying to say that the claimed load instruction has nothing to do with access of the memory ? access level includes, and not limited to, at least determination of the memory address and the loading of the data from memory.

14. As to b) above, applicant is reminded that unclaimed feature cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite "must calculate", or

"must not calculate" , or the like. Applicant only claims "without requiring computation" (see claim 1, lines 3-4).

15. Applicant taught clearly instructions that store and load from an identical offset from an identical register are determined to be referencing the identical memory location, without having to actually compute the physical target address (page 3, lines 18-22, page 4, lines 1-4) . Further, applicant taught a bypass for generating a signal to indicate to a computation stage 130 for not to compute the actual effective address based on the determination of the same address (see page 9, lines 9-11, lines 13-22). The actual effective address is the base address and the offset address (see page 8, lines 10-11). The offset is a partial address. No address other than the effective address which was not calculated could be found in the specification by examiner. Therefore, reading claim in view of specification, the "without computation of ...memory address" is interpreted as "without computation of ...actual effective address".

16. Amerson disclosed a system for determining the same address by comparing the partial or complete address referenced by the load instruction with store address (e.g. see col.8, lines 13-54). The comparison was done based on the overlapping of the partial memory address, therefore, no calculation of the actual effective address was needed in comparison. The partial address was used in comparison to determine the same address by the load and store.

17. As to c) above, Webb disclosed a system including a bypass circuit for comparing the address of a load with the address of a recent store, and if match occurs the store provided the data instead of retrieving data from the memory (e.g. see col.4, lines 43-48, see col.6, lines 10-15). Therefore, no calculation of the actual effective address to the memory was needed because the retrieval from the memory was avoided. If the retrieval from the memory was avoided, the actual effective address of the memory must not have been calculated. The data was provided from the internal store instead from the memory (see also the bypass in col.7, lines 21-25).

18. Claims 6-11, 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the detection of the load and store instructions of identical locations in a pipelined microprocessor by examining the symbolic structure of instructions.

19. Claims 20 , 21 are allowable over the art of record for reciting detailed functional operations of the syntax determination and the respective first and second memory locations.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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